



Improved parameter targeting in 3D-integrated superconducting circuits through a polymer spacer process

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Abstract

Three-dimensional device integration facilitates the construction of superconducting quantum information processors with more than several tens of qubits by distributing elements such as control wires, qubits, and resonators between multiple layers. The frequencies of resonators and qubits in flip-chip-bonded multi-chip modules depend on the details of their electromagnetic environment defined by the conductors and dielectrics in their vicinity. Accurate frequency targeting therefore requires precise control of the separation between chips and minimization of their relative tilt. Here, we describe a method to control the inter-chip separation by using polymer spacers. With the spacers, we measure a mean tilt of $(76 \pm 36) \mu\text{rad}$, and a mean deviation of $(0.4 \pm 0.8) \mu\text{m}$ from the target inter-chip separation of $10 \mu\text{m}$. We apply this process to coplanar waveguide resonator samples and observe chip-to-chip resonator frequency variations below 50 MHz ($\approx 1\%$). We measure internal quality factors of 5×10^5 at the single-photon level, suggesting that the added spacers are compatible with low-loss device fabrication.

Keywords: Three-dimensional integration; Flip-chip bonding; Superconducting microwave resonators; Coplanar Waveguide or CPW; Frequency targeting; Quality factor

1 Introduction

Quantum computing shows immense promise for enabling simulations of complex many-body quantum systems for materials science and quantum chemistry [1]. Solving realistic problems will require hundreds or thousands of nearly perfect quantum bits (qubits) [2], necessitating scalable implementations. Superconducting circuits are one leading implementation for qubits that fulfill this criterion [3]. Due to finite qubit coherence times and control accuracy, quantum error correction, based, for example, on the surface code [4, 5], will be needed, requiring millions of physical qubits (depending on qubit error rates and noise model assumptions) [2, 6, 7]. Fabricating this quantity of qubits remains a formidable engineering challenge and will require innovative techniques such as flip-chip bonding to combine multiple planar (single-layer) chips [8–10] and superconducting

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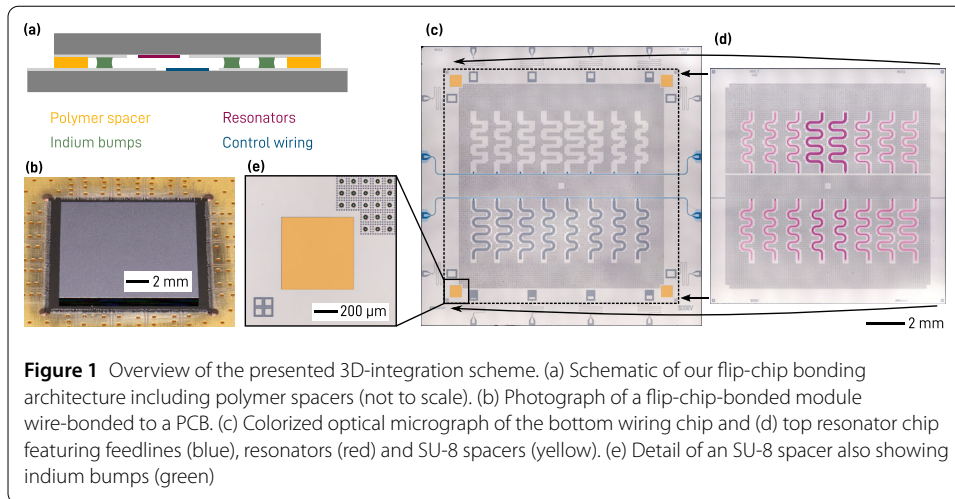
through-substrate vias to suppress package modes [11, 12]. While air-bridge [13, 14] crossings can overcome some routing challenges [15], planar devices will remain limited to a maximum routing density set by the acceptable crosstalk between closely spaced signal traces [16]. Instead, the multi-chip approach will ultimately prove more fruitful since circuit elements (qubits, couplers, readout resonators, *etc.*) can be placed on separate chips which have optimized fabrication procedures or even different material platforms [17, 18].

In flip-chip bonding, two patterned devices are joined face-to-face by bumps of superconducting metal, typically indium due to its ductility and facile cold-welding [8–10]. The inter-chip spacing, d , is a key parameter since it affects the frequencies of resonant features, the impedance matching between different signal lines, and the capacitive and inductive coupling rates between elements (such as for qubit–qubit couplers or the qubit–readout resonator coupling) [19]. Values of d between 5 μm and 10 μm are typical, with smaller separations increasing the inter-chip capacitance (*cf.* a parallel-plate capacitor) and hence the coupling rates at the expense of increased electric field redistributions (compared to planar designs) that change device parameters like the phase velocity of transmission lines [20].

Relative chip tilt is problematic for 3D-integrated devices since it leads to local changes in the chip-to-chip separation, d , and hence to local frequency shifts of device components. Since indium is soft, compression during flip-chip bonding can result in significant tilt. An investigation by Foxen *et al.* found 500 μrad of tilt for an indium-based flip-chip bonding process, which corresponds to 6 μm of separation difference across a 12 mm chip, a large fraction of the chip separation [10]. This leads to predicted local frequency shifts of several hundred MHz (several %) for coplanar-waveguide (CPW) resonators when using typical dimensions (discussed in Appendix A). The anticipated errors will be even larger for resonator coupling rates to qubits [19] or the feedlines used for readout multiplexing since the rates depend on higher powers of the coupling capacitance.

To avoid the tilt or deviation of the chip separation compared to the target value, Niedzielski *et al.* and Li *et al.* have demonstrated hard-stop spacers which mechanically support the chip [21, 22]. Silicon spacers [21] are ideal from a process-compatibility perspective, but uniformly etching large silicon wafers without increasing surface roughness or loss rates is a significant fabrication challenge. Alternatively, large indium pads [22] can act as spacers by significantly increasing the indium surface area and diluting the bonding force. Such indium pads are simple to define during the usual indium bump deposition process but their height can be difficult to control due to the substantial thickness being deposited. Recently, Somoroff *et al.* have detailed a hybrid approach, where, instead of using separate indium bumps and hard spacers, they have used bumps composed primarily of aluminum with a thin coating of indium [23]. This process saves the space required for dedicated spacers but still suffers from the difficulty of evaporating thick films with precise thicknesses. Therefore, we chose to develop a spacer process based on SU-8, which has previously been used in situations where galvanic connections are not required [24, 25]. Favorable properties of SU-8 spacers include: a simple fabrication process, suitability for wafer-scale processing, compatibility with standard fabrication procedures for low-loss devices, excellent height uniformity, and independent control over the chip separation.

Here, we present this SU-8 spacer process for indium flip-chip bonding. In Sect. 2, we specify our device architecture and fabrication details. Then, we analyze the impact of the SU-8 spacers on inter-chip spacing and tilt in Sect. 3. Next, we discuss the frequency



reproducibility of resonators on devices with spacers in Sect. 4, before analyzing the quality factors of the resonators as a function of their geometric parameters in Sect. 5 and concluding in Sect. 6.

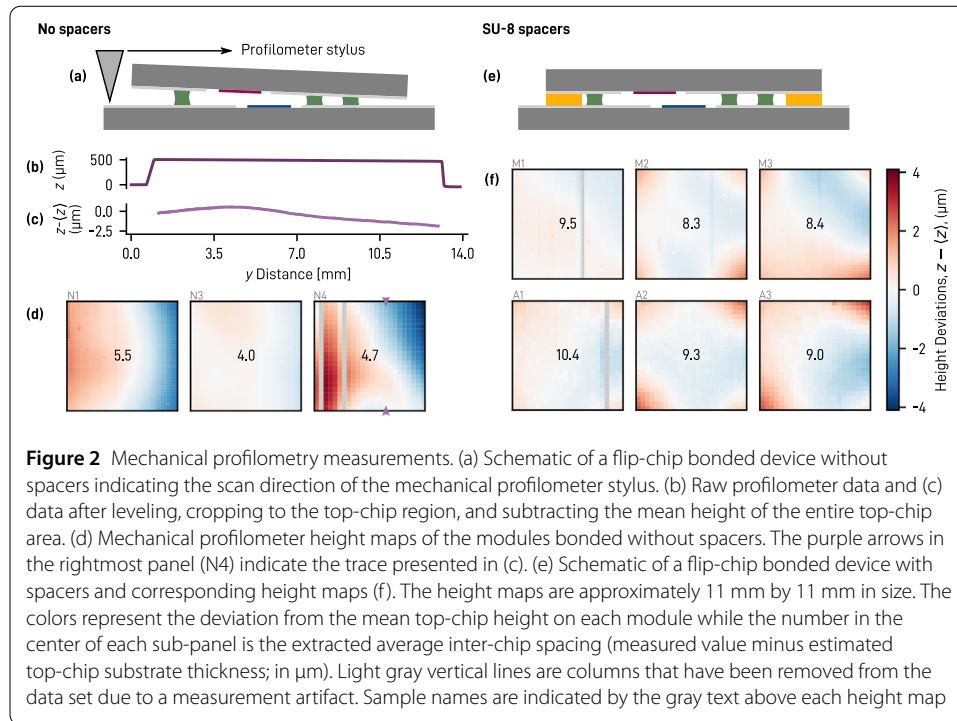
2 Device architecture and fabrication

Our multi-chip module [Fig. 1(a,b)] comprises a resonator chip (top) bonded to a wiring chip (bottom) with a target inter-chip separation of 10 μm . Here, the wiring chip [Fig. 1(c)] includes the multiplexed feedlines and wire-bond connections to the break-out printed-circuit board (PCB) while all resonators are on the top resonator chip [Fig. 1(d)]. Superconducting indium bumps (25 μm diameter, 10 μm thickness) mechanically support the resonator chip and galvanically join the ground planes of the two chips to suppress spurious modes. 600 μm by 600 μm by 10 μm pads of SU-8 photoresist in the corners of the overlap area on the bottom wiring chip support the resonator chip during bump bonding and act as a mechanical stop to ensure uniform chip separation [Fig. 1(e)]. Larger versions of the optical micrographs are provided in Appendix B.

We fabricate these devices on 100 mm high-resistivity ($> 20 \text{ k}\Omega \text{ cm}$) silicon wafers onto which we sputter 125 nm of niobium before patterning the film with SF_6 -based reactive ion etching. Afterwards, we pattern 10 μm of SU-8 3010 photoresist on the wiring chips to act as spacers. Next, we pattern a negative photoresist, thermally evaporate 10 μm of indium on both the wiring and resonator chips, and then remove the unwanted indium by dissolving the photoresist under it in a solvent bath, lifting it off. After dicing, we flip the resonator chip, align it with the wiring chip using a split-prism microscope inserted between the two chips, and then bond them by compressing the indium bumps against each other at room temperature. This compresses the $\approx 20 \mu\text{m}$ of indium across both bumps by a factor of two down to around 10 μm . To perform microwave measurements, we glue the device to a sample package and wire bond it to a PCB. For additional details about the fabrication process, see Appendix B.

3 SU-8 spacer performance

To comprehensively inspect the inter-chip separation, we use mechanical profilometry, where, as depicted in Fig. 2(a), a stylus is drawn linearly across the sample while recording the deflection, resulting in a height vs. position line scan [Fig. 2(b)]. We observe a step of



just greater than $500\ \mu\text{m}$ from the upper surface of the bottom chip to the upper surface of the top chip, corresponding to the substrate thickness of the top chip plus the chip separation. We level the data based on the bottom chip and select only the top chip region, resulting in a trace [Fig. 2(c)] with a smoothly varying profile, with some tilt and bow (curvature), and with total deviations from the mean of around $3\ \mu\text{m}$.

Performing a series of such line scans, and processing the data as discussed above, we prepare the height maps presented in Fig. 2(d,f). All measurements were performed with the device in the same orientation [that depicted in Fig. 1(c)], and this attitude has been preserved during plotting and analysis. Some line scans in the height maps are offset downwards by $\approx 1\ \mu\text{m}$ from adjacent ones due to measurement artifacts in the profilometer; using a procedure described in Appendix C, we remove (mask) these traces, resulting in the gray vertical lines in Fig. 2(d,f). Note that, for plotting, we subtract the mean height of the entire top-chip region for the data displayed in Fig. 2(c,d,f). Furthermore, we point out that this technique cannot distinguish chip separation from thickness variations of the top chip substrate. Independently, we measure the standard deviation of our wafer thicknesses at $1.0\ \mu\text{m}$ or below (discussed further in Appendix C).

In devices without spacers [Fig. 2(d)], we observe large tilts as evidenced by the color gradient as well as deviations relative to the mean of $\pm 4\ \mu\text{m}$. Once spacers are added [Fig. 2(f)], tilts are substantially reduced and there are no longer large chip-separation gradients from one side of the sample to the other. Instead, now that large tilts are avoided, we observe bowing, with the corners raised by roughly $1\ \mu\text{m}$ and the center depressed by slightly less than that.

For quantitative analysis [and the text values in Fig. 2(d,f)], we subtract the estimated top-chip substrate thickness (from independent measurements; see Appendix C). We observe a mean separation of $(5.8 \pm 1.9)\ \mu\text{m}$ (mean \pm standard deviation) over four devices without spacers and $(9.6 \pm 0.8)\ \mu\text{m}$ for nine devices with spacers, which is closer to the tar-

get separation and has reduced variation compared to the spacerless devices. We compute the tilt for these chips by fitting a plane to the data using a least-squares method, convert this to standard θ , ϕ spherical coordinates, and average over θ to find a mean tilt of $(284 \pm 166) \mu\text{rad}$ for the spacerless devices and $(76 \pm 36) \mu\text{rad}$ for the devices with spacers. The remaining height maps, data processing methodology, sample details, and further analysis of the tilt are presented in Appendix C. Thus, based on our analysis, the spacers improve the centering of the process, bringing the chip separations closer to target and reducing tilts as well as suppressing variance in both parameters (particularly worst-case results). While centering issues might be improved for spacerless devices by adjusting bonding parameters, the SU-8 spacers help to center the process automatically without additional parameter sweeps and investigation.

Furthermore, to enable comparisons to published results [22, 24, 26], we have also measured the chip-to-chip separation at the corners of the top chip with scanning electron microscopy (SEM). While chip separation information in the middle of the sample is not available without destructive techniques, we find quantitative agreement with the corners of the profilometer height maps. More details about the SEM measurements and the results are presented in Appendix C.

Here we note that SU-8 spacers require some special care since they absorb common solvents used for resist stripping and swell up, necessitating special drying procedures and reducing the height uniformity compared to the heights immediately after spinning, developing, and baking (discussed in Appendix B). Comparing our measured data to literature values, the relative deviations from the target height are similar to those reported for silicon [21] and indium [22] spacers, although the silicon spacers reported yet smaller tilts (calculated from spacer heights prior to bonding rather than measured on bonded devices). Additionally, while the separation and tilt errors of current spacerless processes [26] have improved compared to early reports [10], they are still larger than for processes with spacers. Thus, despite minor fabrication issues, SU-8 performs comparably in practice to indium and silicon spacers.

The bowing apparent in Fig. 2(f) is a concern since it could replace tilt as the dominant source of local frequency errors. The observed bowing could be the result of the geometry of the flip-chip bonder, elastic compression of the SU-8 spacers which leads to inelastic compression of the indium,¹ and the current layout of spacers located only at the edges of the resonator chip. The flip-chip bonder and spacer placement can easily be adjusted, but compression of the SU-8 requires adapting to lower-force indium bonding or replacement by a less-compressible spacer material.

4 Resonator frequency targeting

Having shown that the SU-8 spacers improve our chip separation and planarity targeting, we next verify that this results in reproducible parameters for microwave circuits. In particular, we investigate resonator frequencies since they are important for fast, multiplexed readout circuits [27] in which readout resonators must be matched to Purcell filters within tens of MHz ($\approx 0.5\%$ relative accuracy).

¹The Young's modulus of SU-8 is nearly two orders of magnitude smaller than that of silicon.

While standard planar CPWs have electrical properties ideally determined entirely² by the permittivity of the substrate and the ratio, $w/(w + 2s)$, between the center conductor width, w , and the gap width, s , the electrical properties of 3D-integrated CPWs depend additionally on the layout of conducting and dielectric features on, and the distance, d , to the opposite chip [20]. Typical planar CPWs have center conductor widths, $w \approx 10 \mu\text{m}$ [28], greater than or equal to the attainable chip separations, d , with evaporated indium bumps. Since the impedance changes are particularly acute when $w \gtrsim d$, we utilize a smaller $w = 5 \mu\text{m}$ and adapt the gaps on either side, s , to target a 50Ω impedance. This balances reduced precision of lithographic processes, increased kinetic inductance [29], and increased losses due to the greater electric field strength [30] against separation-dependent properties and compactness.

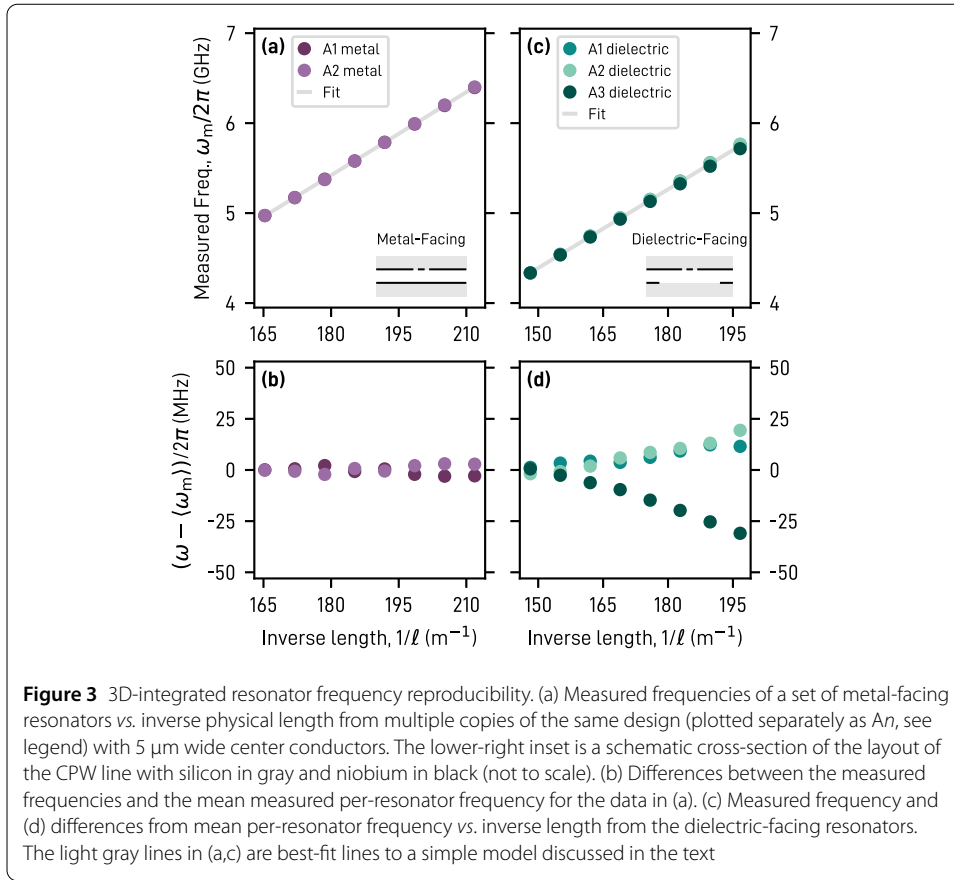
In addition, we can cover the chip opposite the CPW with varying amounts of metal, which will change the boundary conditions for the electric field and hence influence the microwave properties (phase velocity and losses); see Appendix A for concrete examples and discussion of the limiting cases. To our knowledge, the behavior as a function of material facing the CPW has been simulated [31] but has not been investigated experimentally to date in this context. Here, we compare resonators on the top chip facing a solid metal film on the bottom chip in the region opposite the CPW (*metal facing*) and resonators where the metal has been etched away during device fabrication in a $140 \mu\text{m}$ wide strip centered across from the CPW to expose the dielectric beneath (*dielectric facing*). For dielectric-facing devices, we leave small strips of metal ($\approx 10 \mu\text{m}$ wide) in this etched region to connect the ground planes and avoid spurious modes; see Fig. 1(c) and the device design renders in Fig. 10 for more information.

We designed samples with two feedlines of eight weakly coupled quarter-wavelength CPW resonators with frequencies staggered in 200 MHz increments from 4.5 GHz to 6.5 GHz and coupling quality factors of approximately 2×10^6 . One feedline features metal-facing CPWs while the other has dielectric-facing CPWs, see Fig. 1(c). Since the feedline is located on the wiring chip while the resonators are on the other chip, we couple them with inter-chip parallel-plate capacitors. Further details about the sample designs are available in Appendix D.

We cooled the resonators down to approximately 15 mK in a dilution refrigerator and measured the complex scattering parameters of the resonators with a vector network analyzer (VNA). Additional information about the measurement setup is available in Appendix E. We extracted the resonator frequency at a drive power which provides good signal-to-noise ratio and where the resonator does not show nonlinear behavior using a fitting technique which is robust to impedance mismatches [32].

In a first measurement, we verify that the fundamental resonance frequency scales with the physical length of the resonator using a sample (design A) with $5 \mu\text{m}$ -wide CPW center conductors. For the simplest case (the metal-facing resonators), we plot the measured resonance frequencies against the inverse physical length, $1/\ell$, of the resonator in Fig. 3(a) and observe a linear scaling. This indicates that these CPWs behave as expected, with a resonant frequency given by $v_{\text{ph}}/4\ell$ where v_{ph} is the effective phase velocity of this particular geometry and dielectric. We fit the mean per-resonator measured frequency to a simple

²Assuming that the CPW dimensions are significantly smaller than the substrate thickness and distance to any metallic enclosure.



analytical model that accounts for the additional frequency shift due to the coupling to the feedline (presented in Appendix F) by a least-squares method and extract a phase velocity of $v_{\text{ph},m}^{\text{fit}} = 1.182 \times 10^8$ m/s for this geometry. This v_{ph} may be process specific, since the phase velocity of a CPW will depend on details such as the metal film thickness, the degree of over-etching of the substrate, or oxide films on the various surfaces.

Furthermore, we analyze the reproducibility of the measured frequencies by comparing the nominally identical resonators on two or three copies of this design. We plot the difference between the measured frequencies and the mean of all measured frequencies of each resonator on the sample in Fig. 3(b) and observe a standard deviation of 4 MHz or $\approx 0.05\%$ between the same resonators on different copies of the device (16 resonators on two devices). This indicates excellent reproducibility for the metal-facing CPW geometry.

Next, we investigate the case of CPWs with a 5 μm-wide center conductor and dielectric facing the CPW line. We again find frequencies proportional to $1/\ell$ [Fig. 3(c)] and fit a phase velocity of $v_{\text{ph},d}^{\text{fit}} = 1.175 \times 10^8$ m/s. For these resonators, we observe a standard deviation between different copies of the same resonator of 16 MHz [Fig. 3(d); 24 resonators on three devices]. This deviation is dominated by copy A3 which had slightly damaged spacers (for reasons discussed in Appendix B) and a rightward tilt with a magnitude twice as large as that of the other two copies [samples A1, A2, and A3 were also measured by mechanical profilometry and their height maps are plotted in order from left to right in the lower row of Fig. 2(f)]. Since the resonators decrease in length from left to right along each feedline, the rightward tilt of the top chip on copy A3 is expected (see Fig. 5) to shift

the frequency of the shorter resonators downward more than the longer ones, as observed in Fig. 3(d). Excluding this device, we calculate a standard deviation of 4 MHz across 16 resonators on two devices.

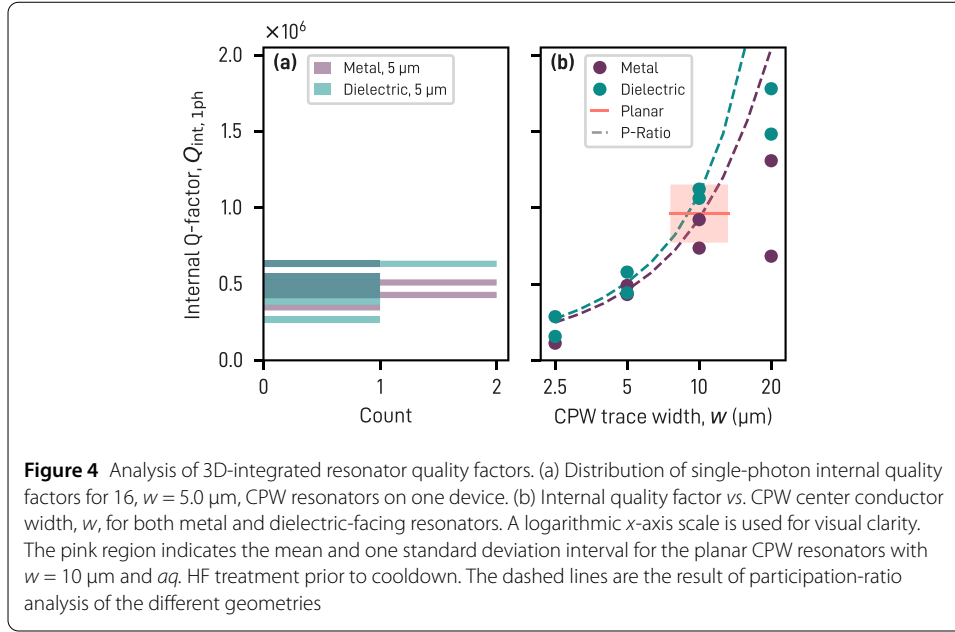
Combining the results of both metal- and dielectric-facing resonators, we find a frequency difference standard deviation 16 MHz and a maximum difference between two nominally identical resonators of 50 MHz (4 MHz standard deviation and 8 MHz maximum difference when excluding sample A3). For similar 3D-integrated devices without spacers, we find a standard deviation of 4 MHz and a maximum difference of 17 MHz (32 dielectric-facing resonators on two devices), while for planar devices fabricated using similar methods but without spacers or indium bumps, we find a mean frequency difference standard deviation of 16 MHz and a maximum frequency difference of 59 MHz within a single wafer or 23 MHz and 64 MHz across wafers (28 resonators on eight devices spread over three wafers).

Although these data for devices with spacers are from a single fabrication round, they show comparable frequency reproducibility to devices without spacers, indicating that the spacer process itself does not worsen frequency reproducibility. Furthermore, since the frequency reproducibility of the devices with spacers is below typical wafer-to-wafer frequency variations from planar devices, the flip-chip bonding process is not expected to limit the frequency repeatability of weakly coupled CPW resonators. Resonators with larger coupling capacitors may show greater sensitivity to inter-chip spacing deviations since the spurious capacitances to ground that shift the frequency (see Appendix F) will depend on d . For 3D-integrated devices, the frequency targeting is expected to be confounded by inter-chip separation deviations or tilt (see Fig. 5) but here the reduced variation observed in devices with spacers should limit this effect.

Given good frequency reproducibility, it is useful to model the phase velocity of such resonators to target specific frequencies in future designs. Typical approaches include analytical techniques such as conformal mapping [20, 33, 34] or finite-element (FEM) simulations [26]. We find that conformal mapping calculates phase velocities of $v_{\text{ph},m}^{\text{CM}} = 1.215 \times 10^8$ m/s ($v_{\text{ph},d}^{\text{CM}} = 1.185 \times 10^8$ m/s) for the metal-facing (dielectric-facing) CPWs while 3D radio-frequency (RF) FEM simulations produce phase velocities of $v_{\text{ph},m}^{\text{FEM}} = 1.233 \times 10^8$ m/s ($v_{\text{ph},d}^{\text{FEM}} = 1.205 \times 10^8$ m/s). These values are within 5% of the measured values in the worst case, and a large portion of the remaining error is likely attributable to kinetic inductance [29, 35]. In general, accurately modeling the absolute frequencies of CPW resonators is challenging due to: (i) geometrical effects resulting from fabrication such as the metal thickness and the over-etch into the substrate; (ii) kinetic inductance of the Cooper pairs in the superconductor which depends on the film thickness and penetration depth; and (iii) parasitic effects missing in the equivalent model. Complicating matters further, (i) and (ii) may vary spatially across the wafer.

5 Resonator quality factors

Having analyzed the reproducibility of resonator frequencies and modeled them, we next evaluate the impact of the additional process steps introduced for the 3D-integrated samples on the low-photon number internal quality factors of the CPW resonators. Quality factors at this power are important since this is a standard benchmark and the regime in which qubits are operated [36]. For the $w = 5 \mu\text{m}$ CPWs, we find a mean internal quality factor at single photon levels, $Q_{\text{int},1\text{ph}}$, of $(0.5 \pm 0.1) \times 10^6$, with no statistically



significant difference between metal-facing and dielectric-facing resonators [Fig. 4(a)]. This is comparable to 3D-integrated devices without spacers, where we observe $Q_{\text{int,1ph}} = (0.5 \pm 0.1) \times 10^6$ over 16 dielectric-facing resonators with $w = 4 \mu\text{m}$. We provide the internal quality factor data as a function of internal photon number for all samples in Appendix G and discuss the calculation of the resonator internal photon number in Appendix H.

Considering a second sample (design B) where the CPW center conductor width is set to $2.5 \mu\text{m}$, $5 \mu\text{m}$, $10 \mu\text{m}$ and $20 \mu\text{m}$ for different resonators while adapting the gap size to approximately maintain a 50Ω impedance according to the conformal mapping model (resulting in proportionally larger gaps at large w), we observe that the internal quality factors are strongly affected by CPW size, scaling by a factor of ≈ 5 from $w = 2.5 \mu\text{m}$ to $w = 20 \mu\text{m}$ [Fig. 4(b)]. We expect larger w and gaps to reduce the field strength and thus the participation of lossy interfaces, resulting in increased quality factors. Indeed, the observed dependence agrees qualitatively with numerical participation-ratio analysis of the geometries (discussed in Appendix I). Importantly, the $w = 10 \mu\text{m}$ resonators have $Q_{\text{int,1ph}} \approx 1 \times 10^6$, which is comparable to $Q_{\text{int,1ph}} = (1.0 \pm 0.2) \times 10^6$ in airbridge- and qubit-free, hydrogen-fluoride (HF) treated planar resonators with identical w produced in our lab using similar fabrication techniques but without SU-8 spacers or indium bumps. Thus, the SU-8 spacer process does not limit resonator quality factors at this level and the 5×10^5 quality factors reached by the $w = 5 \mu\text{m}$ resonators on both the A and B samples are likely limited by our decision to use a smaller w compared to planar designs to reduce the sensitivity of transmission line properties on chip separation rather than additional steps in the 3D integration process.

6 Discussion

To improve parameter reproducibility of indium flip-chip bonded superconducting microwave circuits, we have developed an SU-8 spacer process. We showed that the spacers reduce the mean chip separation error to a mean of $(0.4 \pm 0.8) \mu\text{m}$ and tilt to a mean of

$(76 \pm 36) \mu\text{rad}$. Furthermore, we demonstrated the ability of the profilometry technique to characterize the entire bonded area by uncovering bowing which is not visible with SEM measurements of the chip corners or pre-bonding measurements of the spacer heights. Additional investigation of such bowing is required, particularly the impact of additional spacers. SU-8 spacers have advantages due to the simplicity and accessibility of their fabrication process. Based on our measurements, SU-8 spacers perform comparably to silicon and indium spacers. However, further study will be needed to evaluate their qubit compatibility and the best approach, particularly given their propensity for absorbing solvents during standard cleaning steps used in state-of-the-art qubit fabrication.

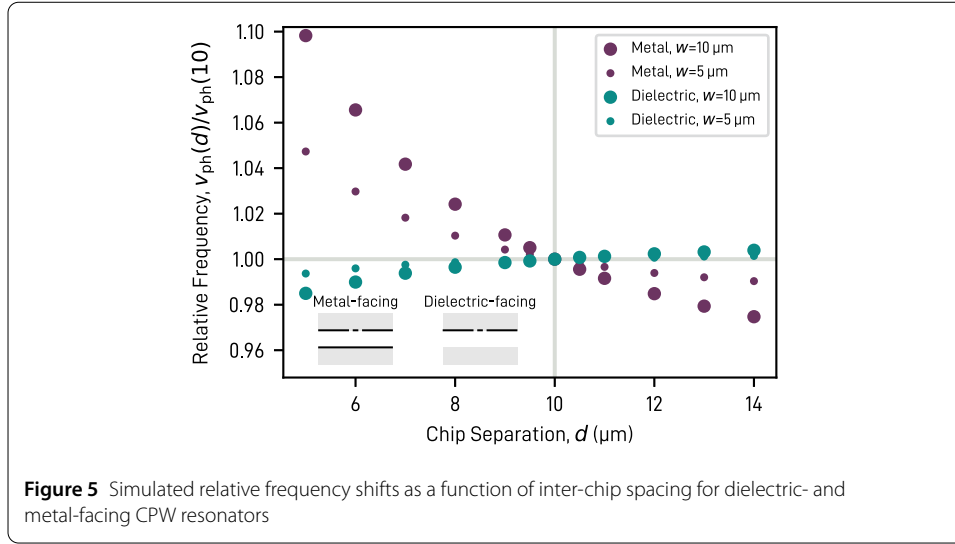
We also verified that the reproducible chip separation results in CPW resonator frequencies with statistical device-to-device frequency deviations below the typical wafer-to-wafer variations, which should enable multiplexed readout circuits including Purcell filters in future work. For 3D-integrated CPWs with a $5 \mu\text{m}$ -wide center conductor, we found that standard techniques do not model the phase velocities with sufficient precision for *ab initio* device design and will need to be refined in future studies, particularly by investigating kinetic inductance in these geometries. Future work could also intentionally vary the height of the SU-8 spacers to correlate frequency shifts with inter-chip separation, which would also help to improve our models.

Measurements of the resonator quality factors show that the flip-chip bonding process preserves the low-loss material interfaces of a similar planar fabrication process at the level of quality factors of 5×10^5 . Resonators with wider center conductors reached higher internal quality factors in exchange for potentially increased sensitivity to chip separation deviations. We did not find significant differences between metal- and dielectric-facing resonators, indicating that we can use either based on design convenience. In particular, due to their reduced phase velocity sensitivity on chip spacing deviations, dielectric-facing resonators may be preferred at the cost of physically longer resonators due to their lower phase velocity. More work is needed to investigate alternative geometries (microstrip-like) to avoid the quality-factor penalties of narrow CPW lines and preserve separation-independent properties.

Appendix A: Frequency dependence on chip separation

Since it is challenging to accurately produce a sequence of chips over a large range of target separations, we turn to simulations to numerically explore the influence of chip separation on the frequency of CPW resonators. We consider a center conductor width, w of $10 \mu\text{m}$ and gaps of $5.5 \mu\text{m}$ to ground on either side on top of $525 \mu\text{m}$ of silicon with a relative permittivity, $\epsilon = 11.45$ [37], and assume that there is either a $525 \mu\text{m}$ thick piece of silicon (dielectric-facing) or a sheet of metal (metal-facing) a distance d away on the opposite chip. We calculate the phase velocity, $v_{\text{ph}}(d)$ using 3D RF FEM simulations and plot the relative frequency shift of a resonator as the ratio $v_{\text{ph}}(d)/v_{\text{ph}}(10 \mu\text{m})$ in Fig. 5.

The dielectric-facing CPW resonator shifts downwards in frequency with decreasing chip separation due to the increasing electric field participation in the dielectric (increasing the effective permittivity ϵ_{eff} and lowering v_{ph}). The metal-facing CPW resonator shifts upwards in frequency with decreasing chip separation due to the increasing electric field participation in the vacuum region between the center trace and the metal film above (increasing v_{ph}). Decreased chip separation relative to the target value results in larger



deviations than increased separation, and metal-facing CPWs experience far larger frequency shifts with changing d than dielectric-facing ones due to the different boundary conditions.

In both cases, we see that $< 1 \mu\text{m}$ deviations around the target distance of $10 \mu\text{m}$ result in frequency changes below 1%, but large negative deviations ($\approx 5 \mu\text{m}$) result in frequency shifts of at least a few percent or hundreds of MHz for resonant frequencies around 5 GHz.

Furthermore, we have simulated CPWs with $w = 5 \mu\text{m}$ and gaps of $3.24 \mu\text{m}$ ($3.14 \mu\text{m}$) for the metal-facing (dielectric-facing) resonators, which show reduced frequency shifts with changing d compared to the $w = 10 \mu\text{m}$ CPWs, motivating our choice of $w = 5 \mu\text{m}$ for the devices in this work.

The absolute phase velocities for the $w = 5 \mu\text{m}$ CPWs at $d = 10 \mu\text{m}$ are presented in the main text. For the $w = 10 \mu\text{m}$ CPWs at $d = 10 \mu\text{m}$, we calculate $v_{\text{ph},\text{m}}^{\text{FEM}} = 1.275 \times 10^8 \text{ m/s}$ ($v_{\text{ph},\text{d}}^{\text{FEM}} = 1.190 \times 10^8 \text{ m/s}$) for the metal-facing (dielectric-facing) CPWs.

We recently became aware of another work [31] that also simulates 3D-integrated CPW resonator frequencies as a function of inter-chip separation and whether the resonators are metal- or dielectric-facing. Li *et al.* found similar shifts using finite-element and conformal mapping techniques and propose a spacing-insensitive design mixing metal- and dielectric-facing regions on a single resonator.

Appendix B: Fabrication details

B.1 Niobium deposition and patterning

We fabricate the devices discussed in this work on 100 mm, (100)-orientation, high-resistivity ($> 20 \text{ k}\Omega \text{ cm}$) intrinsic float-zone silicon wafers (*Topsil GlobalWafers A/S*). We clean the wafers for 5 min in a 1 : 1 mixture of 25% ammonium hydroxide (NH_4OH) and 30% hydrogen peroxide (H_2O_2) at 60°C to remove organic contaminants before stripping the native silicon oxide for 60 s in a 7% solution of hydrofluoric acid (HF) in water at room temperature and then rinsing with de-ionized (DI) water. Within 20 min, we place the cleaned wafers into the load-lock of an ultra-high-vacuum (base pressure $< 1 \times 10^{-7} \text{ Pa}$) magnetron sputtering system (*AJA International Inc.*), where we sputter $\approx 125 \text{ nm}$ of niobium from a 100 mm niobium target (99.99%, *ACI Alloys, Inc.*) in a face-to-face geometry

over 300 s with a 25 sccm flow of Ar resulting in a chamber pressure of ≈ 1 Pa. Before venting to the atmosphere, we expose the fresh niobium film to nitrogen gas for 15 min.

After unloading the wafer, we clean it with sonication in a 50°C bath of isopropanol to remove particles before spinning AZ 5214E (EU) photoresist (*Microchemicals GmbH*) (45 s of spinning at 4000/min followed by a 60 s bake at 105°C on a hotplate). We expose the wafers in contact mode with a mask aligner (*EV Group*, EVG 620NT) at an exposure dose of 60 mJ/cm² of an even mix of 365 nm, 405 nm and 420 nm light-emitting-diode (LED) illumination. After exposure, we develop the resist for 60 s in AZ 726 MIF (*Microchemicals GmbH*) followed by 60 s of rinsing in DI water and a spin rinse and dry. We etch the now-exposed niobium film in a reactive-ion etcher (*Oxford Instruments*, Plasmalab 80 Plus) using SF₆ chemistry, a chamber pressure of 9×10^2 Pa, a flow rate of 5 sccm, and an RF power of 100 W for approximately 240 s using the reflectivity of the surface to a helium-neon laser to determine the end of the etch. We strip the resist for at least 120 min in 80°C *N*-Methyl-2-pyrrolidone (NMP) followed by 10 min NMP, acetone, and then isopropanol sonication at 50°C.

After stripping, we measure step heights from the niobium surface to the silicon below of approximately 155 nm in the center of the wafer increasing to 185 nm at the edge of the wafer using mechanical profilometry. Using our measured niobium thickness of approximately 125 nm in the center of the wafer, this indicates over-etches into the silicon of approximately 30 nm in the center and 60 nm at the edge of the wafer.

B.2 SU-8 patterning

Before starting the patterning of the SU-8, we clean the wafers for 60 s in a 7% HF solution at room temperature and then rinse with DI water. We spin SU-8 3010 (*Kayaku Advanced Materials, Inc.*) for 60 s at 3000/min and then allow the film to rest for 5 min on the spinner before soft baking for 180 s at 95°C. We expose the SU-8 on a mask aligner (EVG 620NT) in contact mode at an exposure dose of 200 mJ/cm² of 365 nm LED illumination and perform post-exposure bakes at 65°C for 60 s and then 300 s at 95°C on a vacuum hotplate. We develop for 90 s in mr-Dev 600 and then wash several times in alternating isopropanol and mr-Dev 600 baths until no residues remain. To improve the mechanical resilience of the SU-8 spacers, we next hard bake at 180°C for 900 s. Finally, we perform mechanical profilometer (*Bruker Corp.*, DektakXT) measurements of the niobium and SU-8 thicknesses.

We note that, since the baking temperature of typical electron-beam-lithography (EBL) resists used for Josephson junction fabrication are above the melting temperature of indium (156°C), EBL needs to be performed prior to indium deposition.

B.3 Indium patterning

Before starting the indium patterning, we clean the wafers for 60 s in a 7% HF solution at room temperature (45 s for wafers with SU-8) and then rinse with DI water. We start by spinning AZ nLOF 2070 (*Microchemicals GmbH*) for 1 s at 3000/min with 1 s ramps on either side before allowing the wafer to rest on the spinner for 300 s with the lid open. Then, we soft bake for 30 s at 100°C before removing the edge bead with a few mL of propylene glycol methyl ether acetate (PGMEA) while spinning at 500/min and then 30 s at 1500/min once the PGMEA has been applied. We bake for 360 s at 100°C on a vacuum hotplate and then expose on a mask aligner (EVG 620NT) in contact mode at an exposure dose of 110 mJ/cm² of an even mix of 365 nm, 405 nm and 420 nm LED illumination. Next,

we perform a post exposure bake at 110°C for 60 s on a vacuum hotplate before developing in AZ 826 MIF (*Microchemicals GmbH*) for 90 s and then rinsing in DI water. We then load the wafer into a thermal evaporator (*Plassys Bestek*, ME450S-In) and perform an *in-situ* argon ion mill for 300 s at a beam voltage of 500 V, a beam current of 35 mA, and an argon flow of 6 sccm. Without breaking vacuum, we evaporate $\approx 10\ \mu\text{m}$ of indium at 10 nm/s with the wafer temperature held at approximately 4°C in a water-cooled chuck. To complete the indium deposition, we lift-off the indium on top of the resist film in 50°C acetone over 120 min.

B.4 Dicing, cleaning, and SU-8 drying

With the indium patterning completed, the individual dies are finished. To prepare for dicing, we spin AZ 4533 (*Microchemicals GmbH*) resist for 60 s at 1000/min before baking for 90 s at 80°C to protect the front surface of the wafer. After dicing, we clean individual chips with isopropanol and acetone to remove the resist followed by 15 min in 80°C NMP to remove resist residues, then 60 min in 50°C acetone and bake for at least 12 h in a vacuum oven at 50°C and $2 \times 10^4\ \text{Pa}$ to remove the solvents from the SU-8 spacers.

Immediately after spinning, exposure, development, and baking, the mean SU-8 3010 spacer height is $(10.00 \pm 0.04)\ \mu\text{m}$. However, after immersing in warm solvents (in particular, NMP), the SU-8 spacers increase in thickness up to 25%, which we counteract with a solvent-exchange and drying procedure (detailed above). Immediately prior to bonding, the SU-8 spacer height is approximately $(10.2 \pm 0.2)\ \mu\text{m}$.

If used within several weeks of fabrication, the SU-8 spacers are robust to the cleaning procedure described above. After sitting under protective photoresist for several months, many of the spacers partially or fully delaminate during NMP cleaning. A short acetone and isopropanol cleaning may be used in this case, although this could affect the resulting internal quality factors.

B.5 Flip-chip bonding and packaging

Then we flip-chip bond the bottom and top chips together in a flip-chip bonder (*Smart Equipment Technology Corp. SA*, FC150). The bonder uses an autocollimator to ensure that the bottom and top chips are parallel prior to bonding and a split-prism microscope inserted between the chips to align them laterally. We calibrate the parallelism of the arm and chuck, align the autocollimator, and finally align the microscope so that it points to the same locations on the chuck and arm. After inserting the chips, we align the bottom and top chips in five axes (lateral position and rotation as well as the two rotation axes for parallelism) and press them together at room temperature with a force between 10 N/mm² to 40 N/mm² of indium (20 N/mm² typical). Unlike Ref. [10], we do not use atmospheric plasma cleaning to remove the indium oxides prior to bonding. We discuss the available information we have on our bump-bond galvanic connection yield in Appendix J.

After flip-chip bonding, we glue (GE 7031 Varnish) the module onto an oxygen-free high thermal conductivity (OFHC) copper base with a microwave printed circuit board (PCB) attached. Next, we connect launchers on the PCB and bottom chip using a manual wedge-type wire bonder (*West Bond, Inc.*, 7476E) with 25 μm diameter aluminum wire. Finally, we close the sample package with a 6082 aluminum alloy lid and vacuum bag the sample for transport from the cleanroom to the laboratory where it is installed in a cryostat.

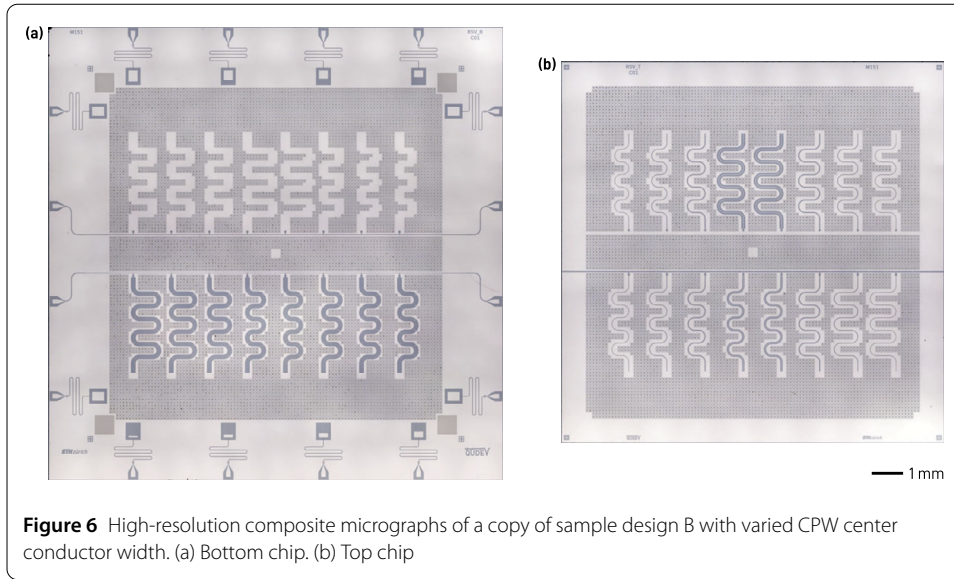


Figure 6 High-resolution composite micrographs of a copy of sample design B with varied CPW center conductor width. (a) Bottom chip. (b) Top chip

B.6 Additional imagery

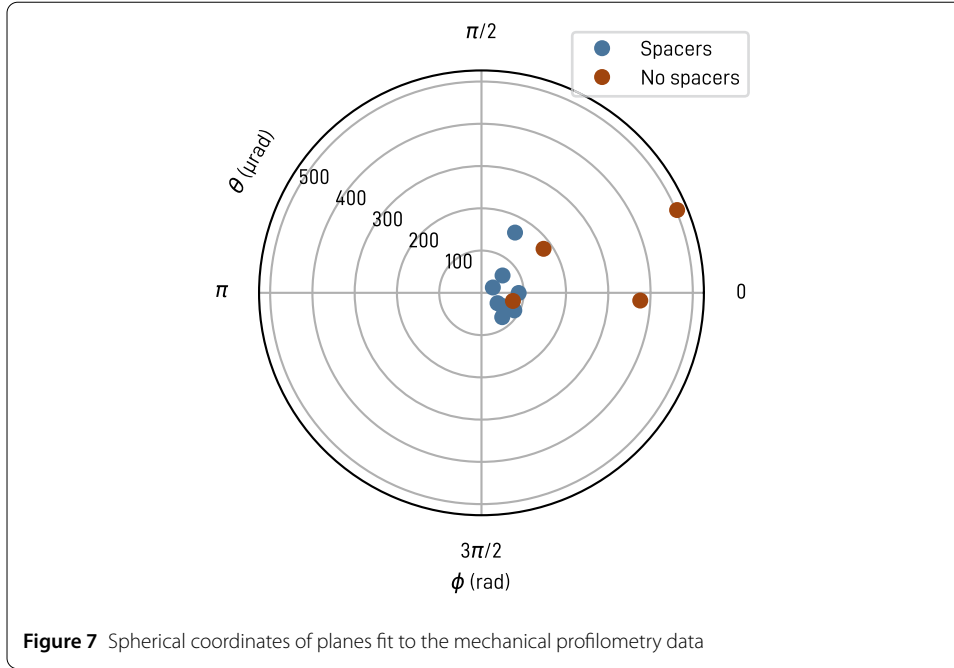
We present additional composite micrographs of a copy of the design B with varied CPW center conductor width in Fig. 6. These composite images have been created by aligning and merging numerous images taken with a microscope including corrections for lighting non-uniformity (Hugin) before performing curve adjustments to increase contrast (GNU image manipulation program). The micrographs in the main text [Fig. 1(c,d,e)] are desaturated versions of these micrographs which have been artificially colored.

Appendix C: Mechanical measurements

C.7 Mechanical profilometry

We measure each bonded module in the mechanical profilometer (*Bruker Corp.*, DektakXT) starting from the lower-right corner of the bottom chip. The dektak scans first vertically from bottom to top and then repeats such scans from the right edge of the bonded device until the left edge. We level the data by fitting a plane to bottom chip region in the complete dataset with a least-squares method and then subtracting this plane from the entire dataset.

Next, we subtract the substrate thickness from the measured top-chip heights. We first estimate the thickness of the substrates by accurately measuring the thickness of other wafers from the same batches using a precision micrometer (*Mitutoyo Corp.*, MDH-25MB). We used two different types of wafers for these devices: double-side polished for the mechanical test samples, and single-side polished for the resonator samples. We find that our double-side polished wafers have a mean thickness of $(505.9 \pm 1.0) \mu\text{m}$ and that our single-side polished wafers have a mean thickness of $(525.2 \pm 0.4) \mu\text{m}$. We thus crop the data to just the top-chip region and subtract the appropriate substrate thickness to arrive at the extracted chip separations. Finally, we mask out (remove) individual vertical line scans where the mean finite difference from column n to $n + 1$ is greater than $0.5 \mu\text{m}$, corresponding to the artifacts where the mechanical profilometer has measured an entire line scan lower than the adjacent ones.



We fit a plane, $-ax - by - c + z = 0$ to the estimated chip-separation data using a least-squares procedure with the following equation: $A\vec{v} = \vec{z}_{\text{meas}}^T$, where A is a $[\vec{x}_{\text{meas}}^T, \vec{y}_{\text{meas}}^T, \vec{1}^T]$ and $\vec{v} = [a, b, c]^T$. The normal vector to this plane is given by $\hat{n} = \vec{w}/\|\vec{w}\|$ with $\vec{w} = [-a, -b, 1]$. We convert this normal to spherical coordinates following ISO convention

$$r = \|\vec{n}\| = 1 \quad (\text{C.1})$$

$$\theta = \arccos\left(\frac{\hat{n}[3]}{r}\right) \quad (\text{C.2})$$

$$\phi = \text{sgn}(\hat{n}[2]) \arccos\left(\frac{\hat{n}[1]}{\sqrt{\hat{n}[1]^2 + \hat{n}[2]^2}}\right). \quad (\text{C.3})$$

A two-dimensional plot of these data (Fig. 7) shows a clear bias towards the right which may be a result of our particular flip-chip bonder and calibration procedure. The mean values reported in the main text in Sect. 3 are the average value of θ . Since the data is not centered around the origin, the non-negative aspect of θ should not confound the comparison of mean θ values discussed in the main text.

The remaining height maps are presented in Fig. 8, and the device parameters and analysis results are given in Table 1.

C.8 Scanning-electron microscopy

We image the corners of the top chip of a bonded device edge-on with two different detectors in the scanning-electron microscope (SEM) and measure the gaps manually using changes in contrast to detect the bottom-chip and top-chip edges (see Fig. 9). Since the bottom-chip edge is visible only by differences in local contrast due to depth-of-focus, there is some ambiguity in these measurements which we attempt to reduce by using two different detectors. Additionally, since we are only within a few degrees of perpendicular to the edge, we estimate that these measurements have an uncertainty of a few hundred

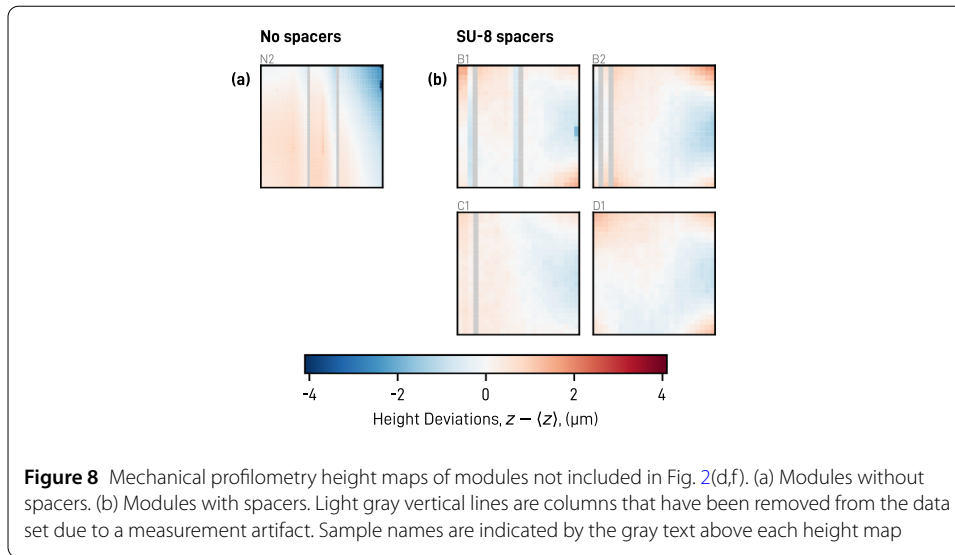
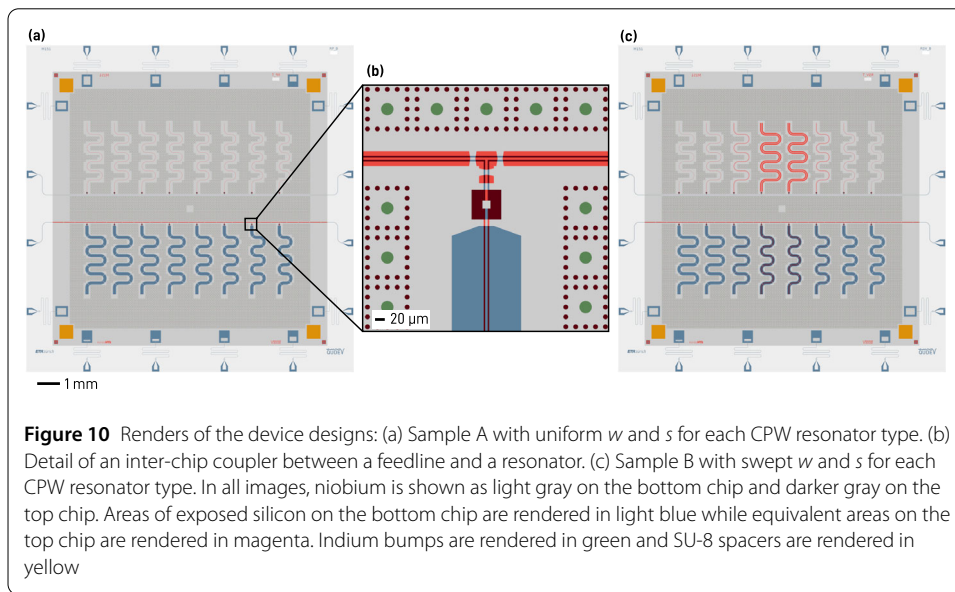
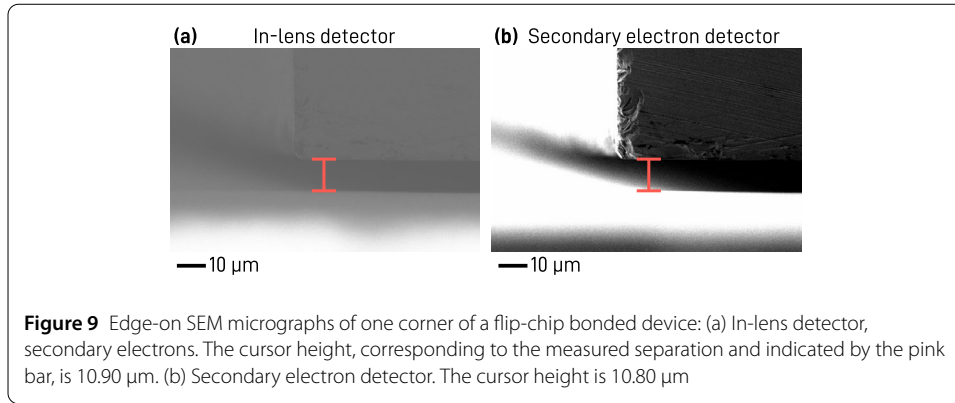


Table 1 Mechanical measurement results. Samples A1 through M3 have spacers unless noted otherwise. Samples N1 through N4 have no spacers. p_b : bonding pressure, $c - t_{w,est}$: fit plane height minus estimated wafer thickness (from independent measurements), θ : fit plane polar angle, ϕ : fit plane azimuthal angle

Name	p_b (N/mm ²)	$c - t_{w,est}$ (μm)	θ (μrad)	ϕ (rad)	Note
A1	20	10.37	88.0	5.79	Partially delaminated spacers
A2	20	9.32	57.7	5.72	
A3	20	9.01	160.9	5.83	
B1	20	10.09	45.2	5.71	
B2	20	9.68	74.7	5.77	
C1	20	10.72	88.0	6.28	
D1	20	10.18	75.7	5.42	
M1	10	9.54	64.6	0.69	
M2	20	8.30	29.7	0.44	
M3	40	8.39	163.2	1.06	
N1	20	5.51	376.1	6.23	
N2	10	8.89	180.1	0.62	
N3	20	3.98	76.9	6.03	
N4	40	4.69	502.6	0.40	

nm. We then average the chip separations from both detectors into a single value for that corner. The average separation for the module is the mean of the corner separations. To compute the tilt, we utilize the methodology of Ref. [26], *i.e.* we compute the inverse tangent of the chip separation difference divided by the lateral distance for all six corner pairs on the device and quote the largest value. A tilt extracted from fitting a plane to the measured data is typically lower than these worst-case local tilts.

Without spacers, we calculate a mean per-module corner separation of $(6.1 \pm 0.2) \mu\text{m}$ and mean per-module worst-case tilt of $(450 \pm 200) \mu\text{rad}$ across four bonded modules. This calculation is similar to that of Ref. [26] and we find comparable, although slightly worse, values. With spacers, we extract a separation of $(11.0 \pm 0.3) \mu\text{m}$ and a tilt of $(62 \pm 26) \mu\text{rad}$ over nine modules. All devices in Table 1 excluding sample A3 are included in this



set of nine devices. We find that the corner separations extracted from SEM measurements are consistent with the mechanical profilometry. The larger inter-chip separation results from the SEM method are likely caused by the observed bowing.

Appendix D: Sample details

All results in this work are based on 14.3 mm by 14.3 mm bottom chips and 12.0 mm by 12.0 mm top chips. We present renders of the resonator sample device designs in Fig. 10. For the mechanical tests, additional samples with a uniform array of bumps and no CPWs were used. Devices with SU-8 spacers have four 600 μm by 600 μm rectangles of SU-8 placed on the bottom chip just within the outline of the top chip. They are sized such that, assuming a Young's modulus of 2 GPa [38], we expect a compression of only 7% when using a bonding force of 200 N.

The indium bumps are 10 μm high, 25 μm diameter, and have a pitch of 100 μm . The samples have a total number of bumps ranging from 8297 to 11,096, resulting in a total area of between 4 mm² and 5.4 mm² of indium.

The dimensions of the CPW resonators for sample design A are listed in Table 2. The resonators are coupled to the feedline with parallel-plate capacitors made of overlap-

Table 2 CPW resonator parameters of design A. Resonator indices increase from left to right along the feedline; 0 to 7 refer to the metal-facing resonators on the upper feedline while 8 to 15 refer to the dielectric-facing resonators on the lower feedline. w : center conductor width, s : gap width, ℓ : physical length, $\langle\omega_m\rangle$: mean measured resonance frequency

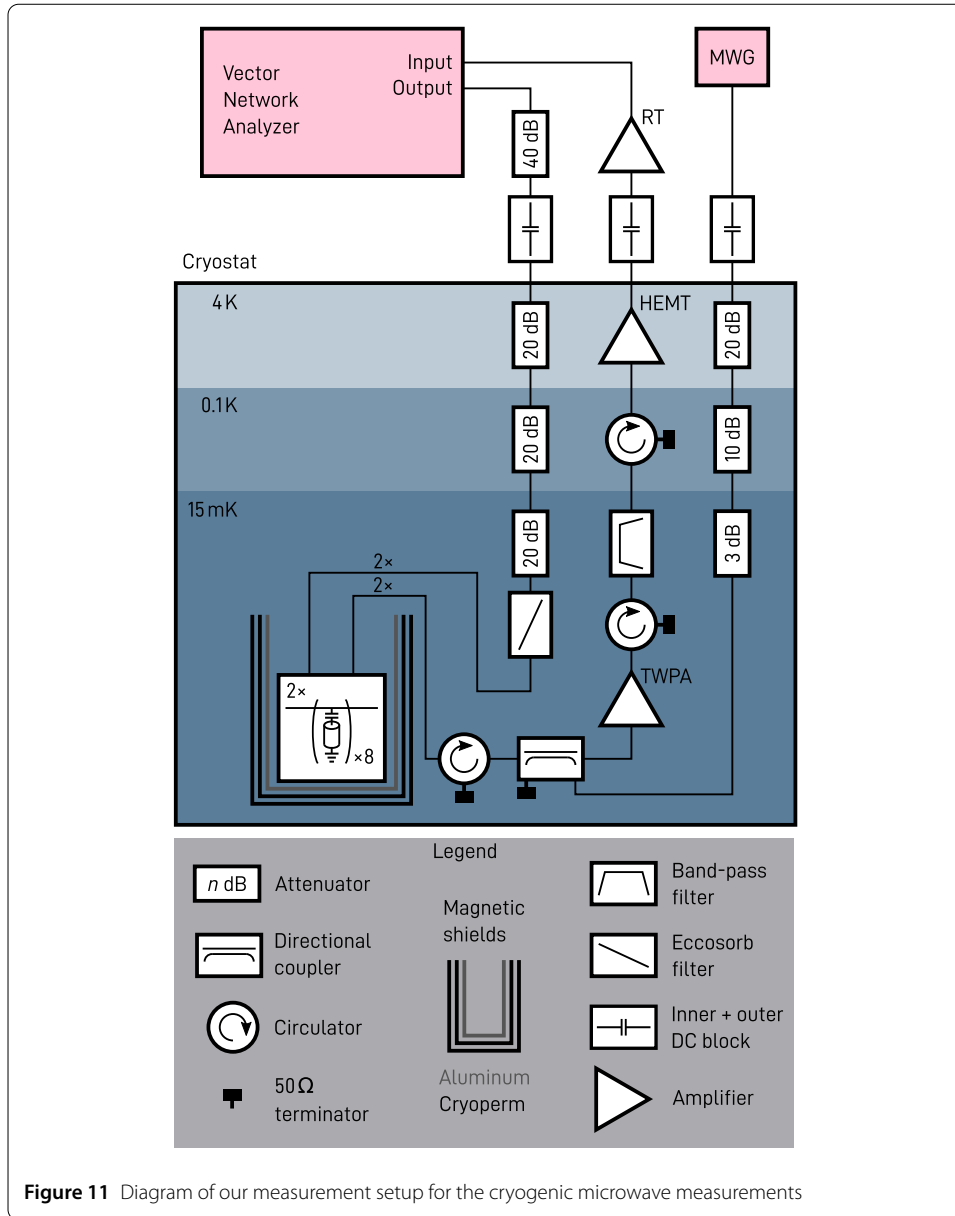
Index	w [μm]	s [μm]	ℓ [μm]	$\langle\omega_m\rangle/2\pi$ [GHz]
0	5.00	3.24	6049.8	4.9729
1	5.00	3.24	5816.1	5.1724
2	5.00	3.24	5599.7	5.3748
3	5.00	3.24	5398.7	5.5797
4	5.00	3.24	5211.6	5.7865
5	5.00	3.24	5037.0	5.9921
6	5.00	3.24	4873.7	6.1990
7	5.00	3.24	4720.5	6.3988
8	5.00	3.14	6749.1	4.3347
9	5.00	3.14	6447.9	4.5386
10	5.00	3.14	6172.4	4.7407
11	5.00	3.14	5919.4	4.9423
12	5.00	3.14	5686.2	5.1448
13	5.00	3.14	5470.6	5.3458
14	5.00	3.14	5270.7	5.5467
15	5.00	3.14	5082.8	5.7475

ping $16\text{ }\mu\text{m}$ by $16\text{ }\mu\text{m}$ square pads with a uniform $22\text{ }\mu\text{m}$ gap to ground on all sides [see Fig. 10(b)]. In electrostatic simulations (*Ansys, Inc.*, Maxwell 2022 R1, discussed in more detail in Appendix K), we compute a capacitance of approximately 0.44 fF between the pads, and surplus capacitances to ground (compared to a coplanar waveguide of the equivalent length) of approximately 0.6 fF on the resonator and feedline side. We define the physical length of the resonators, ℓ , to start from the center of the square coupling capacitor pad.

Appendix E: Microwave measurement setup

The signal path (see Fig. 11) begins at a vector network analyzer (*Agilent Technologies*, N5230C) before passing through a 40 dB attenuator and then an inner and outer DC block. The cryostat (*Bluefors Oy*, LD250) features further 20 dB attenuators at the 4 K, 100 mK, and 15 mK stages of the input line before a final custom coaxial Eccosorb filter (*Laird plc.*, Eccosorb CR-110). The reasoning behind this choice of attenuators is presented in Ref. [39]. The sample is enclosed in a package with a copper base and aluminum lid and then placed inside a high-purity aluminum magnetic shield surrounded by two high permeability nickel-alloy shields (*Magnetic Shields Ltd.*, Cryophy). The output line features an isolator (*Low Noise Factory*, ISIS4_12A), a 20 dB directional coupler, a traveling wave parametric amplifier (TWPA) (*MIT Lincoln Labs*), another LNF isolator, and then a band-pass filter on or below the base temperature stage. The output line then has an additional circulator at the 100 mK stage and a high-electron mobility transistor (HEMT) amplifier (*LNF*, LNC4_8A) at the 4 K stage. Outside the cryostat, the output line has an inner and outer DC block and the room-temperature amplification chain consisting of: an ultra-low-noise amplifier (ULNA), a low-pass filter, a 10 dB attenuator, a low-noise-amplifier (LNA), a 3 dB attenuator, and another inner and outer DC block.

Our measurements were performed without pumping the TWPA (*i.e.* with it off) to avoid saturation effects at high probe powers and frequency-dependent gain that might distort the resonator lineshapes.



Appendix F: Analytical resonator model

Here, we analyze an electrical model of a CPW resonator capacitively coupled to a feedline to determine the resonant frequency under this additional loading and to find a model to extract the CPW phase velocity from resonator frequency measurements as a function of resonator length. As shown in Fig. 12, we consider our resonator as a quarter-wavelength ($\lambda/4$) transmission line of impedance $Z_{0,r}$ and bare resonance frequency ω_0 connected to a two-ended feedline of impedance $Z_{0,f}$ by a coupling capacitance C_c . We include a parasitic capacitance to ground C_{cgr} (C_{cgf}) on the resonator (feedline) side and expect that the spurious capacitance to ground on the resonator side will lower the resonant frequency.

We write out the total impedance of the circuit about the selected node (the blue dot in Fig. 12) and extract the loaded resonant frequency from the poles of this impedance. Setting $C_{cgf} = 0$ to simplify notation (it only contributes at high order) and assuming

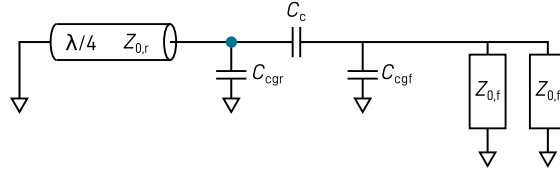


Figure 12 Circuit representation of the coupling circuit between the $\lambda/4$ resonators and the feedline

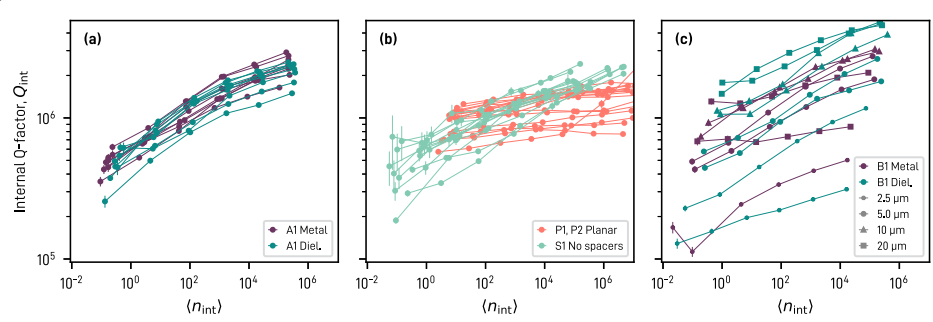


Figure 13 Resonator internal quality factor as a function of internal photon number. (a) Sample A1. (b) Planar (P1 and P2) samples as well as a 3D-integrated sample without spacers (S1). (c) Sample B1. Vertical bars at each point represent the uncertainty of the fit

$(C_c Z_{0,f} \omega/2)^2$ is small, we find the resonance condition:

$$\tan\left(\frac{\pi}{2} - \frac{\ell}{v_{ph}} \frac{\omega_r}{2\pi}\right) - (C_c + C_{cgr})Z_{0,r}\omega_r = 0 \quad (\text{F.1})$$

where we have substituted $\omega_0 = v_{ph}/4\ell$ for a $\lambda/4$ resonator with phase velocity, v_{ph} , and physical length ℓ . Assuming that the capacitive frequency shift is small, so $\omega_r \approx \omega_0$, we can expand the tangent and arrive at a solution for ω_r :

$$\omega_r = \frac{\pi}{2} \frac{1}{\frac{\ell}{v_{ph}} + (C_c + C_{cgr})Z_{0,r}}. \quad (\text{F.2})$$

We fit this model to our measured resonator frequencies using the design lengths (Table 2) with the phase velocity and $b = (C_c + C_{cgr})Z_{0,r}$ as free parameters.

Appendix G: Additional resonator quality factor data

The power dependence of the measured quality factors for devices A1 and B1 discussed in the main text as well as the spacerless control S1 and planar controls, P1 and P2, are presented in Fig. 13.

Appendix H: Resonator internal photon number

We compute the internal photon number of the resonator as a function of applied power using the following formula, which can be easily derived [40]

$$n_{\text{int}} = 2 \frac{\kappa P_{\text{app}}}{\hbar \omega_0 (\kappa + \gamma)^2} \quad (\text{H.1})$$

where κ is the coupling rate to the feedline, P_{app} is the power applied at the input port of the sample, \hbar is the reduced Planck constant, ω_0 is the resonant frequency, and γ is the internal loss rate. We subtract the input line attenuation measured at room temperature from the power supplied by the VNA to arrive at the power applied to the sample input which results in uncertainty of a few dB.

Appendix I: Participation-ratio analysis

To understand the influence of the CPW geometry on losses, we numerically analyze the electric-field distribution, focusing on the fraction of the electric field energy (the *participation ratio*) stored in thin layers on the surfaces of the CPW and substrate representing amorphous surface oxides which are believed to host two-level systems (TLS) that induce loss [36]. This technique is widely used to correlate device geometry with losses and thus quality factors [41, 42].

We partition a two-dimensional, side-cut slice of the chosen CPW geometry into metal, substrate, and vacuum bulk regions as well as metal–substrate (MS), metal–vacuum (MV), and substrate–vacuum (SV) interface regions [41, 43]. We follow standard practice and treat the interface regions as having a thickness of 10 nm and a dielectric constant of $\epsilon = 10$ [41, 43, 44]. We calculate the electric field distribution using an electrostatic solver (*Ansys, Inc.*, Maxwell 2022 R1) configured to perform adaptive meshing steps until the change in participation ratios of the regions outlined above is below 1% from one iteration to the next. We repeat such simulations for all CPW geometries of device B and interpolated values of w in between the measured geometries. See Fig. 14 for a diagram of the different regions considered as well as the final mesh for a $w = 2.5 \mu\text{m}$, $s = 1.49 \mu\text{m}$ CPW line.

Since the participation ratios in the different lossy interfaces are highly correlated (meaning that they scale together with changes in w or s) [44], we are unable to use the calculated participation ratios along with the measured internal quality factors to extract loss tangents of the interfaces (for this, devices with extreme geometries [*e.g.* isotropically etched trenches in the CPW gaps] would be required, as in Ref. [44]). Instead, we follow a simplified procedure to create the participation-ratio curves in Fig. 4, described here. For each geometry, we compute the total interface participation, p_{Σ} :

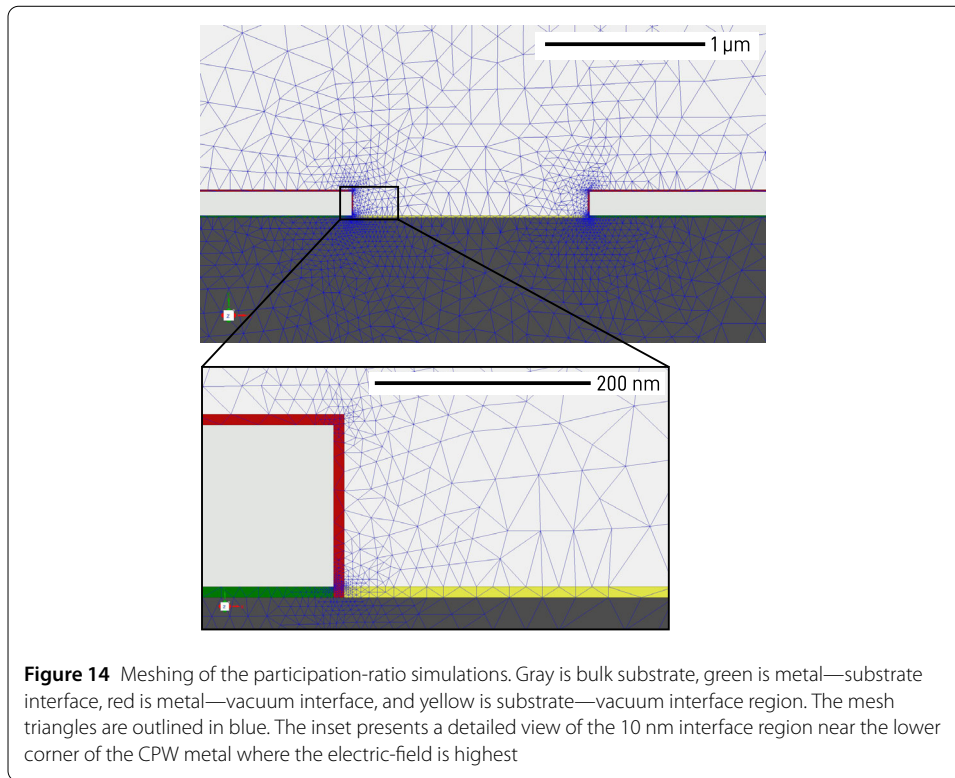
$$p_{\Sigma}(w, x) = \sum_i p_i(w, x) \quad (\text{I.1})$$

where p_i is the participation ratio in one of the three lossy interfaces (MS, MV, or SV), w is the CPW center conductor width, and x is either metal- (m) or dielectric-facing (d). Then, we compute relative Q-factors:

$$Q_{\text{pr}}(w, x) = Q_{\text{meas}}(5 \mu\text{m}, x) \frac{p_{\Sigma}(5 \mu\text{m}, x)}{p_{\Sigma}(w, x)} \quad (\text{I.2})$$

using the mean single-photon internal quality factors for the $w = 5 \mu\text{m}$ resonators of each type on device B.

Compared to the measured data, this procedure overestimates the quality factors at large w , likely since it does not separate the power-dependent (two-level system) and power-independent losses which add in parallel, *e.g.* as done in Ref. [43]. Furthermore,



the participation-ratio curves in Fig. 4 overestimate the quality factors at small w slightly, which could be due to our equal weighting of all interfaces.

Appendix J: Indium bump connection yield

Chains of hundreds or thousands of bumps are typically used to quantify the yield and performance of indium bump galvanic connections [8, 10]. However, these measurements require specific DC measurement equipment.

We have fabricated a sample containing 16 $\lambda/4$ resonators where the shorted end of the resonator is connected to the ground plane only through an indium bump at the current antinode. Thus, the resonator will only be measured at the expected frequency if the indium bump forms a galvanic connection. We find all 16 resonances at the expected frequencies and they have a mean single-photon internal quality factor of $(0.5 \pm 0.1) \times 10^6$. Treating the resonator as a lossless transmission line shorted through a load resistor Z_{In} , we find that a bump resistance of approximately 0.1 m Ω is needed to produce internal quality factors of 0.5×10^6 . Since the physical resonators will have internal loss similar to the device A values, the actual resistance per bump is likely much smaller given the indistinguishable internal quality factors.

Appendix K: Finite-element electrostatic simulations

We simulate the capacitance matrix of the coupling capacitors discussed in this work using a finite-element electrostatic solver (*Ansys, Inc.*, Maxwell 2022 R1). We model each conductor as 125 nm-thick perfect electrical conductor. We assign voltage excitations to the ground planes and capacitor pads and then simulate until the change in total energy

from one iteration to the next is below 0.1% for a minimum of two converged passes. The simulation volume of 1000 μm by 1000 μm by 1060 μm is significantly larger than the ≈ 60 μm capacitor dimensions (*cf.* Section D).

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Abbreviations

3D, three-dimensional; *aq.*, aqueous; CM, conformal mapping; CPW, coplanar waveguide; DC, direct current; EBL, electron-beam lithography; FEM, finite-element method; HEMT, high-electron mobility transistor; HF, hydrofluoric acid; LED, light-emitting diode; LNA, low-noise amplifier; MS, metal-substrate; MV, metal-vacuum; NMP, *N*-methyl-2-pyrrolidone; OFHC, oxygen-free high conductivity; PCB, printed circuit board; PGMEA, propylene glycol methyl ether acetate; qubit, quantum bit; RF, radio frequency; SEM, scanning electron microscope; SV, substrate-vacuum; TLS, two-level system; TWPA, traveling-wave parametric amplifier; ULNA, ultra-low-noise amplifier; VNA, vector network analyzer.

Data availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Ethics approval and consent to participate

Not applicable.

Consent for publication

Not applicable.

Competing interests

The authors declare no competing interests.

Author contributions

G.J.N., J.-C.B., and C.E. planned the experiments. G.J.N. designed and G.J.N. and M.K. fabricated the devices. G.J.N. and D.P. performed the mechanical measurements. G.J.N. performed the microwave measurements and analyzed all data. L.M. performed the participation-ratio analysis. G.J.N. wrote the manuscript with input from all authors. C.E. and A.W. supervised the work.

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